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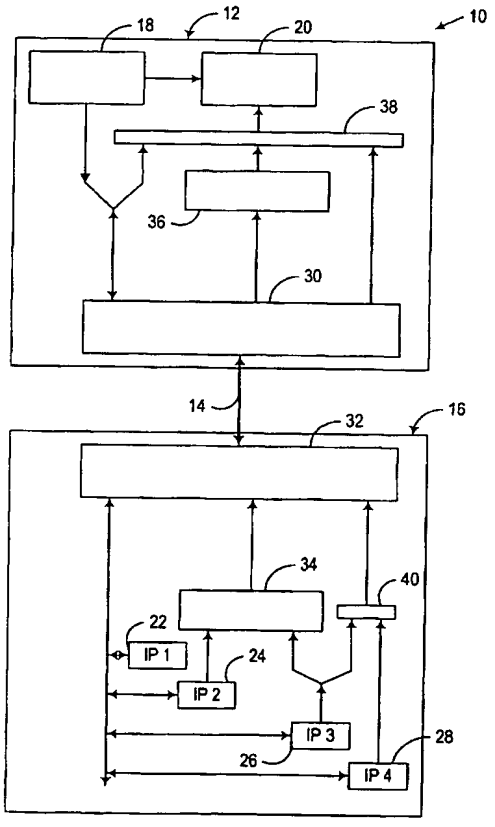
(54) Title: DEDICATED ENCRYPTED VIRTUAL CHANNEL IN A MULTI-CHANNEL SERIAL COMMUNICATIONS INTERFACE



(57) Abstract: A data processing system, circuit arrangement, and method to communicate data over a multi-channel serial communications interface: such as a PCI-express connection (14) using a dedicated encrypted virtual channel from among multiple virtual channels supported by the communications interface (14). Encryption for the dedicated encrypted virtual channel is provided by a hardware encryption circuit (34) that is coupled to the interface, such that encryption may be performed at a relatively low level, and with substantial protection from compromise, particularly along chip boundaries. In one particular application, access control may be provided for a digital data stream using a multi-chip access control scheme that relies on one chip (148) to provide access control over a received digital data stream, with another chip (150) utilized to process the digital data stram once authorized to do so. A secure, multi-channel serial communications interface between the multiple chips re-encrypts a digital data stream that has been decrypted on the access control chip (148) using hardware encryption logic (162) disposed on the access control chip (148), communicates the re-encrypted digital data steam over a dedicated encryption virtual channel supported by the multi-channel serial communications interface, and decrypts the re-encrypted digital data steam using hardware decryption logic (164) disposed on the other chip (150).

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SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:

— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)*

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A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04N5/00 H04N7/24

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, PAJ, WPI Data, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
T	MAYHEW D ET AL: "PCI express and advanced switching: evolutionary path to building next generation interconnects" PROCEEDINGS OF THE 11TH SYMPOSIUM ON HIGH-PERFORMANCE INTERCONNECTS-HOTI'03, 20 August 2003 (2003-08-20), pages 21-29, XP010657970 page 21, left-hand column - page 23, left-hand column page 25, left-hand column, paragraph 2.2.2 ----- -/--	1-45

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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"A" document defining the general state of the art which is not considered to be of particular relevance
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"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.
"&" document member of the same patent family

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Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Carnerero Álvaro, F

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Y	EP 0 875 813 A (SONY CORP) 4 November 1998 (1998-11-04) abstract	2,11-15, 23,32, 41,42, 44,45
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